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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
10/645,800	08/22/2003	Jin Hyung Ryu	HI-0174	9284		
34610	7590	11/14/2008	EXAMINER			
KED & ASSOCIATES, LLP P.O. Box 221200 Chantilly, VA 20153-1200				DINH, DUC Q		
ART UNIT		PAPER NUMBER				
2629						
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/645,800	RYU ET AL.	
	Examiner	Art Unit	
	DUC Q. DINH	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 07 August 2008.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-7 and 13-18 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-7 and 13-18 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on September 08, 2008 has been entered.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claims 1-3 and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art, hereafter, AAPA, pages 1-8 in view of Kumar et al. (U.S Patent No. 5,876,536)

In reference to claim 1 the AAPA discloses in Figs. 3-4 a conventional (page 8, lines 5-6) driving apparatus of a plasma display panel (PDP), comprising:

a multi-chip module (32) in which a plurality of control chips having a control circuit (ASIC 26) for controlling the PDP, and a plurality memories (RAM 33) are mounted on a single package (32), wherein the multi-chip module is mounted on a

printed circuit board (PCB) of a control board (13) [Paragraph 0024] (the original specification discloses control board 13 is a conventional art at paragraph [0026]). The input/output lines coupling the plurality of control chips and the plurality of memories within a single package (32) (**paragraph [0013-0016]**).

The AAPA does not disclose the multi-chip model includes a plurality of green tapes for mounting the control chip and the memory.

Kumar discloses circuit boards are made by casting glass and/or ceramic powders together with an organic powders into tapes, called green are used multilayer circuit board are well known to formed multilayer printed board. (col. 1, lines 14-26)

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to used the green tapes layers as the circuit board for the control chip and memory of the AAPA system as taught by Kumar because it could be used with lower melting, more conductive metals, such as silver, gold and copper for the circuit board to connect the I/O lines connecting the plurality of control chips and plurality of memories (col. 1, lines 35-37 of Kumar).

In reference to claim 2, the AAPA discloses the package is a ball grid type [0022].

In reference to claim 3, the AAPA discloses the multiple chip module transmits a control signal to each driving unit via the PCB (Figs. 3-4; [0021-0022]).

In reference to claim 13, the AAPA discloses a plasma display panel (PDP) driving apparatus comprising:

a control board having a circuit board (13) and a multi-chip module (32) on the circuit board, the multi-chip module including a plurality of control chips (26) and a plurality of memories (33) on a single package (32), the control chip including a control circuit (ASIC) to control a PDP (the original specification discloses control board 13 is a conventional art at paragraph [0026]).

wherein at least one of the plurality of control chips (ASIC) and at least one of the plurality of memories are formed on a front of the circuit package (see Fig. 4) and an input output lines are formed through the plurality of the circuit and the I/O lines connect the at least one control chip and the at least one memory [0024-0025].

The AAPA does not disclose the multiple chip module includes a circuit package having a plurality of circuit layers.

Kumar discloses circuit boards are made by casting glass and/or ceramic powders together with an organic powders into tapes, called green are used multilayer circuit board are well known. (col. 1, lines 14-26)

Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to used the green tapes layers as the circuit board for the control chip and memory of the AAPA system as taught by Kumar because it could be used with lower melting, more conductive metals, such as silver, gold and copper for multi layer the circuit board to connect the I/O lines connecting the plurality of control chips and plurality of memories (col. 1, lines 35-37 of Kumar (col. 1, lines 16-29 and 35-37)

In reference to claim 14, refer to the rejection as applied to claim 2.

In reference to claim 15, refer to the rejection as applied to claim 3.

In reference to claim 16 the AAPA discloses a plurality of driving units to (18 at [0018]) generate and apply driving signals corresponding to control signals received from the control board (13).

In reference to claim 17, the AAPA discloses display (22) to display an image by a plasma discharge based on the driving signals applied from each of the plurality of driving units.

In reference to claim 18, the AAPA discloses wherein the control chip comprises an ASIC type (see claim 7).

4. Claims 4-7 and are rejected under 35 U.S.C. 102(a) as being anticipated by Applicant Admitted Prior Art, hereafter, AAPA, pages 1-8 and Figs. 1-4.

In reference to claim 4, the AAPA discloses a driving apparatus of a plasma display panel, comprising:

a control board (13) provided with a multi-chip module (32) in which a plurality of control chips having a control circuit (26) for controlling the PDP, and a plurality of memories (33) are mounted on a single package (32) the original specification discloses control board 13 is a conventional art at paragraph [0026]).;

a plurality of driving units (18A-18B of Figs. 3-4) for generating and applying a driving signal corresponding to a control signal generated from the control board (13); and a PDP (Fig. 4) for displaying an image by a plasma discharge according to the driving signal applied from each of the plurality of driving units [0020-0025].

wherein the multi-chip module is mounted on a printed circuit board (13) and input/output lines connecting plurality of control chips (26) and a the plurality memories (33) are not formed directly on the PCB (13) but are formed within a single package (32) as shown in Fig. 4 and paragraph [0013-0015]

In reference to claim 5, the AAPA discloses wherein the package is a ball grid type.

In reference to claim 6, the AAPA discloses the control board is provided with a printed circuit board (PCB) on which at least one package is mounted [0024].

In reference to claim 7, the AAPA discloses at least one of the control chips is an ASIC type having a control circuit (Figs. 3-4).

Response to Arguments

5. Applicant's arguments filed on March 07, 2008, have been fully considered but they are not persuasive.

With respect to claims 1 and 4 in which "the control system chips and each of the frame memories are mounted on the PBC as an individual package...", the AAPA paragraphs [0015-0016] disclose the board 32 is implemented in an ASIC type, in which plurality of memories 33 are integrated to form a single package. In addition the system control chip 26 is generally formed by a ball grid type array thereby I/O signal lines connecting the control chips 26 and memories 33 are not formed directly on the PBC but are formed within a single package as claimed. Therefore, the AAPA clearly teaches a multiple chips module (32) in which a plurality of control chips (26) having a control

circuit for control the plasma display, and a plurality of memories (33) are mounted on a single package as in claims 1-4.

With respect to claim 13, refer to the same argument as applied to claims 1-4. In addition, Kumar discloses circuit boards are made by casting glass and/or ceramic powders together with an organic powders into tapes, called green are used multilayer circuit board are well known. (col. 1, lines 14-26). It would have been obvious for one of ordinary skill in the art at the time of the invention to used the green tapes layers as the circuit board for the control chip and memory of the AAPA system as taught by Kumar because it could be used with lower melting, more conductive metals, such as silver, gold and copper for multi layer the circuit board (col. 1, lines 16-29 and 35-37)

In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., control chips and a plurality of memories are mounted on a single package during their fabrication process... and the I/O signal lines does not occupy a wide area; it may be possible to decrease the number of the I/O signal lines...) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

Therefore, the rejection is maintained

Conclusion

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to DUC Q. DINH whose telephone number is (571) 272-7686. The examiner can normally be reached on Mon-Fri from 8:00.AM-4:00.PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Hjerpe can be reached on (571) 272-7691. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Duc Q Dinh/
Primary Examiner,
Art Unit 2629